FACULTY OF ENGINEERING

Scheme of Instruction & Examination

and

Syllabi

B.E. Vand VI Semester

of

Four Year Degree Programme

In

Electronics and Communication Engineering

(With effect from the Academic Year 2018– 2019)
(As approved in the Faculty Meeting held on 26 June 2018)

Issued by

Dean, Faculty of Engineering

Osmania University, Hyderabad

July 2018

SCHEME OF INSTRUCTION & EXAMINATION

B.E. V- SEMESTER

(ELECTRONICS AND COMMUNICATION ENGINEERING)

S. No.	Course Code	Course Title	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
Theory Courses										
1	**PC501EC**	Linear ICs and Applications	3	1	-	4	30	70	3	3
2	**PC502EC**	Analog Communication	3	-	-	3	30	70	3	3
3	**PC503EC**	Digital Signal Processing	3	1	-	4	30	70	3	3
4	**PC504EC**	Automatic Control Systems	3	1	-	4	30	70	3	3
5	**PC505EC**	Computer Organization & Architecture	3	1	-	4	30	70	3	3
6	**PC506EC**	Digital System Design with Verilog HDL	3	-	-	3	30	70	3	3
7	**MC901EG**	Gender Sensitization	3	-	-	3	30	70	3	0
Practical/Laboratory Courses										
8	**PC551EC**	IC Applications lab	-	-	2	2	25	50	3	1
9	**PC552EC**	Systems and Signal Processing Lab	-	-	2	2	25	50	3	1
10	**PC553EC**	Industrial Visit	-	-	-	-	G	-	-	-
Total			**18**	**4**	**4**	**29**	**260**	**590**		**20**

PC: Professional Course **MC**: Mandatory Course

L: Lecture **T:** Tutorial **P**: Practical **D**: Drawing **G**: Grade (E/VG/G/S/U)

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination (Univ. Exam)

Note:

1. Each contact hour is a Clock Hour.
2. The Practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.

Course Code	Course Title						Core / Elective
PC501EC	**LINEAR ICs AND APPLICATIONS**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
AEC (PC401EC)	L	T	D	P			
	3	1	-	-	30	70	3

Course Objectives:

- Describe various configurations of Op-amp.
- Describe the basic principles and practical limitations of Op-amp.
- Describe the various linear and nonlinear applications of Op-amp.
- Describe frequency generators, active filters and voltage regulators.
- Discuss the operation of the most commonly used D/A and A/D converters.

Course Outcomes:

- Illustrate various configurations of Op-amp.
- Illustrate the basic principles and practical limitations of Op-amp.
- Design Linear and Non-linear circuits using Op-amp
- Analyze Frequency generators active filters and voltage regulators.
- Design and analyze ADC & DAC converters.

UNIT - I

Differential Amplifiers: Classification, DC and AC analysis of single / dual input Balanced and unbalanced output Configurations of Differential amplifiers using BJTs, Level Translator.

Operational Amplifier: Ideal, Practical, General (741) bipolar Operational Amplifier, AC and DC performance characteristics, Frequency Compensation, Open-loop and close-loop configurations, 741 Manufacturers data sheet- description, specifications and packages.

UNIT -II

Operational Amplifier Applications-I: Adder, subtractor, Ideal and practical integrator & differentiator, Voltage to current converter, current to voltage converter, differential amplifier, instrumentation amplifier, Log and antilog amplifiers.

UNIT - III

Operational Amplifier Applications -II: Comparator, Precision rectifier, Peak detector, Clippers, Clampers, Sample-and-Hold circuits.

Active Filters Introduction – First order, Second order Active filters – LP, HP, BP, BR and All pass.

UNIT - IV

Waveform Generators: Square wave, Monostable Multivibrator, Schmitt Trigger, saw tooth & Triangular wave generators. Voltage Controlled Oscillator, PLL, NE 555 and its applications. Function Generator –8038.

UNIT - V

Voltage Regulators: Basic of voltage Regulators, Linear regulators using opamp, IC Regulators 78XX and 723.

Data Converters: Introduction, Digital to Analog Converters: Weighted Resistor DAC & Inverted R-2R Ladder DAC. Analog to digital Converters: Parallel Comparator ADC, Successive Approximation ADC and Dual Slope ADC. DAC and ADC specifications.

Suggested Readings:

1. David A Bell, "Operational Amplifiers and Linear ICs," 3/e, Oxford Publications, 2011.
2. Ramakant A. Gayakwad, "Op-Amps and Linear Integrated Circuits," 4/e, PHI, 2010.
3. D.Roy Chowdhury, Shail B.Jain, "Linear Integrated Circuits", 4/e, New / Age International (P) Ltd., 2008.

Course Code	CourseTitle						Core/Elective
PC502EC	**ANALOG COMMUNICATION**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
SATT (PC 304EC)	3	-	-	-	30	70	3

Course Objectives:

1. To analyze the analog communication system requirements
2. To understand the generation & detection of various analog modulation techniques
3. To analyze the noise performance of analog modulation techniques
4. To understand AM and FM receivers
5. To understand the pulse modulation techniques

Course Outcome:

1. Understand analog communication system
2. Compare and analyze analog modulation techniques
3. Calculate noise performance of analog modulation techniques
4. Design AM and FM receivers
5. Differentiate between pulse modulation techniques & continuous modulation techniques.

Unit-I

Linear Modulation schemes: Need for modulation, conventional Amplitude Modulation (AM). Double side band suppressed carrier (DSB –SC) modulation, Hilbert transform, properties of Hilbert transform. Pre-envelop. Complex envelope representation of band pass signals, In-phase and Quadrature component representation of band pass signals. Low pass representation of band pass systems. Single side band (SSB) modulation and Vestigial-sideband (VSB) modulation. Modulation and demodulation of all the modulation schemes, COSTAS loop.

Unit – II

Angle modulation schemes: Frequency Modulation (FM) and Phase modulation (PM), Concept of instantaneous phase and frequency. Types of FM modulation: Narrow band FM and wide band FM. FM spectrum in terms of Bessel functions. Direct and Indirect (Armstrong's) methods of FM Generation. Balanced discriminator, Foster–Seeley Discriminator ,Zero crossing detector and Ratio detector for FM demodulation. Amplitude Limiter in FM.

Unit-III

Analog pulse modulation schemes: Sampling of continuous time signals. Sampling of low pass and band pass signals. Types of sampling. Pulse Amplitude Modulation (PAM) generation and demodulation. Pulse time modulation schemes: PWM and PPM generation and detection. Time Division Multiplexing.

Unit-IV

Transmitters and Receivers: Classification of transmitters. High level and low level AM transmitters. FM transmitters. Principle of operation of Tuned radio frequency (TRF) and super heterodyne receivers. Selection of RF amplifier. Choice of Intermediate frequency. Image frequency and its rejection ratio Receiver characteristics: Sensitivity,Selectivity, Fidelity, Double spotting, Automatic Gain Control.

Unit-V

Noise Sources and types: Atmospheric noise, Shot noise and thermal noise. Noise temperature. Noise in two-port network: noise figure, equivalent noise temperature and noise bandwidth. Noise figure and equivalent noise temperature of cascade stages. Narrow band noise representation. S/N ratio and Figure of merit calculations in AM, DSB-SC, SSB and FM systems,Pre-Emphasis and De-Emphasis.

Suggested Reading:

1. Simon Haykin, "*Communication Systems*," 2/e, Wiley India, 2011.
2. B.P. Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", 4/e, Oxford University Press, 2016
3. P. Ramakrishna Rao, "*Analog Communication*," 1/e, TMH, 2011.

Course Code	Course Title						Core / Elective
PC503EC	**DIGITAL SIGNAL PROCESSING**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
SATT PC 304 EC	3	1	-		30	70	3

Course Objectives:

1. Describe the necessity and efficiency of digital signal processing.
2. Design and implementation of FIR and IIR digital filters.
3. Describe the basics of Multirate digital signal processing and its application.
4. Describe the DSP processor architecture for the efficient implementation of digital filters.

Course Outcomes:

1. Necessity and use of digital signal processing and its application.
2. Analyze FIR and IIR digital filters.
3. Applications of Multirate digital signal processing.
4. Acquaintance of DSP processor and its architecture.

UNIT I:

Discrete and Fast Fourier Transform: Discrete Fourier Transform (DFT), Computation of DFT- Linear and Circular Convolution, FFT algorithms: Radix-2 case, Decimation in Time and Decimation in Frequency algorithms- in place computation- bit reversal.

UNIT II:

Digital Filter (IIR) Design: Butterworth and Chebychev approximation- IIR digital filter design techniques- Impulse Invariant technique- Bilinear transformation technique- Digital Butterworth&Chebyshev filters.

UNIT III:

Digital Filters (FIR) Design: Amplitude and phase responses for FIR filters- Linear phase filters- Windowing techniques for design of Linear phase FIR filters- Rectangular, Bartlett, Hamming, Hanning, Kaiser windows- realization of filters- Finite word length effects, Comparison between FIR and IIR filters.

UNIT IV:

Multirate Digital Signal Processing: Introduction- Decimation by factor D and interpolation by a factor I- Sampling Rate conversion by a Rational factor I/D- Implementation of Sampling Rate conversion- Multistage implementation of Sampling Rate conversion- Sampling conversion by a Arbitrary factor, Application of Multirate Signal Processing.

UNIT V:

Introduction to DSP Processors: Difference between DSP and other microprocessors architecture- their comparison and need for ASP, RISC and CPU- General purpose DSP processors: TMS 320C 54XX processors, architecture, addressing modes- instruction set.

Suggested Reading:

1. Alan V. Oppenheim and Ronald W. Schafer, *"Digital Signal Processing"*, 2/e, PHI, 2010.
2. John G. Praokis and Dimtris G. Manolakis, *"Digital Signal Processing: Principles, Algorithms and Application"*, 4/e, PHI, 2007.
3. Avathar Singh and S. Srinivasan, *"Digital Signal Processing using DSP Micrprocessor"*, 2/e, Thomson Books, 2004.

Course Code	Course Title						Core/Elective
PC504EC	**AUTOMATIC CONTROL SYSTEMS**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
SATT PC 304EC	3	1	-	-	30	70	3

Course Objectives:

1. To Analyze the stability and performance of dynamic systems in both time and frequency domain.
2. To design feedback controllers, such as PID, lead and lag compensators, to meet desired system performance specifications.
3. To provide knowledge of state variable models and fundamental notions of state model design.
4. To understand the classical methods of control engineering and physical system modeling by linear differential equations.
5. To understand state space representation of control systems

Course Outcomes:

1. Convert a given control system into equivalent block diagram and transfer function
2. Analyze system stability using time domain techniques
3. Analyze system stability using frequency domain techniques
4. Design a digital control system in the discrete time domain
5. Analyze a control system in the state space representation.

UNIT – I

Control System fundamentals and Components: Classification of control systems including Open and Closed loop systems,. Transfer function representation: Block diagram representation, Block diagram algebra and reduction and Signal flow graphs and Mason's gain formula.

UNIT – II

Time Response: Transfer function and types of input. Transient response of second order system for step input. Time domain specifications. Characteristic Equation of Feedback control systems Types of systems, static error coefficients, error series,
Stability: Concept of Stability, Routh-Hurwitz criterion for stability, Root locus technique and its construction.

UNIT – III

Frequency response plots: Bode plots, frequency domain specifications. Gain and Phase margin. Principle of argument. Nyquist plot and Nyquist criterion for stability.
Compensation: Cascade and feedback compensation. Phase lag, lead and lag-lead compensators. PID controller.

UNIT – IV

Discrete Control Systems: Digital control, advantages and disadvantages, Digital control system architecture. The discrete transfer function. Sampled data system. Transfer function of sample data systems. Analysis of Discrete data systems.

UNIT – V

State space representation: Concept of state and state variables. State models of linear time invariant systems, State transition matrix, Solution of state equations. Controllability and Observability.

Suggested Reading:

1. Nagrath, I.J, and Gopal, M., "*Control System Engineering*", 5/e, New Age Publishers, 2009
2. Nagoor Kani*.," Control systems*", Second Edition, RBA Publications.
3. Ogata, K., "*Modern Control Engineering*", 5/e, PHI.

Course Code	Course Title						Core/ Elective
PC505EC	**COMPUTER ORGANIZATION AND ARCHITECTURE**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
STLD PC 302 EC	3	1	-	-	30	70	3

Course Objectives:

1. Implement the fixed-point and floating-point addition, subtraction, multiplication & Division.
2. Describe the basic structure and operation of a digital computer.
3. Discuss the different ways of communicating with I/O devices and standard I/O interfaces.
4. Analyze the hierarchical memory system including cache memories and virtual memory.
5. Understand issues affecting modern processors.

Course Outcomes:

1. Perform mathematical operations on fixed and floating point digital data
2. Illustrate the operation of a digital computer
3. Understand I/O interfacing of a computer
4. Interface microprocessor with memory devices
5. Understand latest trends in microprocessors

Unit- I

Data representation and Computer arithmetic: Introduction to Computer Systems, Organization and architecture, evolution and computer generations; Fixed point representation of numbers, digital arithmetic algorithms for Addition, Subtraction, Multiplication using Booth's algorithm and Division using restoring and non-restoring algorithms. Floating point representation with IEEE standards and its arithmetic operations.

Unit-II

Basic Computer organization and Design: Instruction codes, stored program organization, computer registers and common bus system, computer instructions, timing and control, instruction cycle: Fetch and Decode, Register reference instructions; Memory reference instructions. Input, output and Interrupt: configuration, instructions, Program interrupt, Interrupt cycle, Micro programmed Control organization, address sequencing, micro instruction format and micro program sequencer.

Unit-III

Central Processing Unit: General register organization, stack organization, instruction formats, addressing modes, Data transfer and manipulation, Program control. CISC and RISC: features and comparison. Pipeline and vector Processing , Parallel Processing, Pipelining, Instruction Pipeline, Basics of vector processing and Array Processors.

Unit-IV

Input-output organization: I/O interface. I/O Bus and interface modules, I/O versus Memory Bus. Asynchronous data transfer: Strobe control, Handshaking, Asynchronous serial transfer. Modes of Transfer: Programmed I/O, Interrupt driven I/O, Priority interrupt; Daisy chaining, Parallel Priority interrupt. Direct memory Access, DMA controller and transfer. Input output Processor , CPU-IOP communication, I/O channel.

Unit- V

Memory organization: Memory hierarchy, Primary memory, Auxiliary memory, Associative memory, Cache memory: mapping functions, Virtual memory: address mapping using pages, Memory management.

Suggested Reading:

1. Morris Mano, M., "*Computer System Architecture*," 3/e, Pearson Education, 2005.
2. William Stallings, "*Computer Organization and Architecture: Designing for performance*," 7/e, Pearson Education, 2006.
3. John P. Hayes, "*Computer Architecture and Organization*," 3/e, TMH, 1998.

Course Code	Course Title						Core/ Elective
PC506EC	**DIGITAL SYSTEM DESIGN THROUGH VERILOG HDL**						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
STLD PC 302 EC	3	0	-	-	30	70	3

Course Objectives:

1. Describe verilog HDL and develop digital circuits using gate level and data flow modeling
2. Develop verilog HDL code for digital circuits using switch level and behavioral modeling
3. Design and develop of digital circuits using Finite State Machines(FSM)
4. Prepare Algorithmic State Machines(ASM) of Digital design
5. Describes designing with Programmable Logic Devices (PLD's).

Course Outcomes:

1. Appreciate the constructs and conventions of the verilog HDL programming in gate level and data flow modeling.
2. Generalize combinational circuits in behavioral modeling and concepts of switch level modeling
3. Design and analyze digital systems and finite state machines.
4. Comprehend advanced features of verilog HDL and apply them to design complex real time digital system using ASMs
5. Design various circuits for memory devices and annotate the ASIC/FPGA design flow

Unit I

Introduction to HDLs,Overview of Digital Design with Verilog HDL, Basic Concepts, Data types, System tasks and Compiler Directives. Hierarchical modeling, concepts of modules and ports. Gate level Modeling, Dataflow modeling-Continuous Assignments, Timing and Delays. Programming Language Interface.

Design of Arithmetic Circuits using Gate level/ Data flow modeling –Adders, Subtractors**,** 4-bit Binary and BCD adders and 8-bit Comparators.
Verification: Functional verification, simulation types, Design of stimulus block.

Unit II

Switch Level Modeling and examples. Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls, and Conditional Statements, multi-way branching, Loops, Sequential and Parallel blocks, Generate blocks. Tasks and Functions.
Behavioral/dataflow modeling of basic MSI combinational logic modules: ALUs, Encoders, Decoders, Multiplexers, Demultiplexers, Parity generator/checker circuits, Bus Structure.
Basic concepts of Static timing analysis, Logic synthesis

Unit III

Behavioral modeling of sequential logic modules: Latches, Flip Flops, counters and shift registers applications.
Synchronous Sequential Circuits: Analysis and synthesis of synchronous sequential circuits: Mealy and Moore FSM models for completely and incompletely specified circuits,State Minimization-Partitioning Minimization Procedure, sequence detector with verilog HDL modeling.Design of a Modulo-8 Counter using the Sequential Circuit Approach and its verilog implementation. One-Hot Encoding .

Unit IV

Algorithmic State Machines (ASMs):ASM chart, ASM block, simplifications and timing considerations with design example. ASMD chart for binary multiplier and Verilog HDL code, one hot state controller.
Asynchronous Sequential logic: Analysis procedure-Transition table, flow table, race conditions. Hazards with design example of Vending-Machine Controller

Unit V
Introduction to ASIC's: Full-custom, standard-cell and Gate array based ASICs. SPLDs: PROM, PAL, GAL, PLA. FPGA and CPLD simplified architecture and applications. ASIC/FPGA Design flow, CAD tools. Combinational circuit Design with Programmable logic Devices (PLDs).

Suggested Reading:

1. Samir Palnitkar, "Verilog HDL A Guide to Digital Design and Synthesis," 2nd Edition, Pearson Education, 2006.
2. M. Morris Mano, Michael D. Ciletti, "Digital Design", 4th edition, Pearson Education.
3. Michael John Sebastian Smith, *Application Specific Integrated Circuits*, Pearson Education Asia, 3rd edition 2001.
4. Stephen Brown and Zvonko Vranesic,"*Fundamentals of Digital Logic with Verilog Design*",McGraw Hill.

Course Code	Course Title						Core / Elective
MC901EG	**GENDER SENSITIZATION**						Core
Prerequisite	Contact Hours perWeek				CIE	SEE	Credits
	L	T	D	P			
-	3	0	0	0	30	70	0

Course Objectives:

1. To develop students' sensibility with regard to issues of gender in contemporary India.
2. To provide a critical perspective on the socialization of men and women.
3. To introduce students to information about some key biological aspects of genders.
4. To help students reflect critically on gender violence.
5. To expose students to more egalitarian interactions between men and women.

Course Outcomes:

Students will be able to

1. Students will have developed a better understanding of important issues related to gender in contemporary India.
2. Students will be sensitized to basic dimensions of the biological, sociological, psychological and legal aspects of gender. This will be achieved through discussion of materials derived from research, facts, everyday life, literature and film.
3. Students will attain a finer grasp of how gender discrimination works in our society and how to counter it.
4. Students and professionals will be better equipped to work and live together as equals.
5. Students will develop a sense of appreciation of women in all walks of life.

UNIT-I

UNDERSTANDING GENDER:Why Should We Study It? Socialization:Making Women,Making Men: Introduction-Preparing for Womanhood-Growing up male-First lessons in caste-Different Masculinities; **Just Relationships: Being Together as Equals:** Mary Kom and Onler-Love and acid just do not mix-Love Letters-Mothers and Fathers-Further reading: Rosa Parks-The brave heart.

UNIT-II

GENDER AND BIOLOGY: Missing Women: Sex selection and Its Consequences – Declining sex ratio. Demographic Consequences; **Gender Spectrum: Beyond the Binary –** Two or many – Struggles with discrimination; **Our Bodies, Our Health.**

UNIT-III

GENDER AND LABOUR: Housework: the Invisible Labour: "My mother doesn't work"- Share the Load"; **Women's Work; Its Politics and Economics:** Fact and fiction-Unrecognized and unaccounted work- Wages and conditions of work.

UNIT-IV

ISSUES OF VIOLENCE: Sexual Harassment: Say No! : Sexual harassment – not eve-teasing-Coping with everyday harassment-"Chupulu"; **Domestic Violence: Speaking Out:** Is home a safe place? When women unite-Rebuilding lives-New forums for justice; **Thinking about Sexual Violence:** Blaming the victim – "I fought for my life". The caste face of violence.

UNIT – V

GENDER STUDIES: Knowledge - Through the Lens of Gender - Point of view - Gender and the structure of knowledge – Unacknowledged women artists of Telangana: **Whose History? Questions for Historians and Others:** Reclaiming a past-Writing other histories-Missing pages from modern Telangana history.

Suggested Readings:

1. A.Suneetha, Uma Bhrugubanda, Duggirala Vasanta, Rama Melkote, Vasudha Nagaraj Asma Rasheed, Gogu Shyamala, Deepa Sreenivas and Susie Tharu, *"Towards a World of Equals: A Bilingual Text book on Gender"* Telugu Akademi, Hyderabad, 1st Edition, 2015.
2. www.halfthesky.cgg.gov.in

Course Code	Course Title						Core / Elective
PC551EC	**IC APPLICATIONS LAB**						Core
Prerequisite	Contact Hours perWeek				CIE	SEE	Credits
	L	T	D	P			
LICA PC 501EC STLD PC302EC	0	0	0	2	25	50	1

Course Objectives:

- Design and analyze the various linear application of Op-amp.
- Design and analyze the active filters circuit using Op-amp.
- Design and analyze oscillators and Multivibrators using Op-amp & 555.
- Design sequential circuits- Counters &Registers.

Course Outcomes:

- Implement operational amplifiers Linear & Non-linear circuits.
- Implement Active filters using Op-amps.
- Implement oscillators, Multivibrators,etc., using Op-amps.
- Illustrate sequential circuits – Counters & Registers

PART- A

1. Measurement of op-Amp. Parameters, Voltage follower.
2. Inverting and non- Inverting amplifiers using Op-Amp.
3. Integrator Differentiator circuits using Op-Amp.
4. Active filters : LP, HP and BP filters using Op-Amp.
5. Clipper and clamper circuit using Op-Amp.
6. Triangular wave generator using Op-Amp.
7. Monostable and Astable multivibrator using Op-Amp.
8. Monostable and Astable multivibrator using 555 Timer.
9. IC voltage regulator.
10. Voltage controlled oscillator – NE 565
11. Four bit ADC and DAC using Op Amp

PART - B

1. Flip Flop conversions and latches using gates and ICs.
2. Designing Synchronous, Asynchronous up/ down counters.
3. Shift Registers and Ring counters using IC Flip-Flop & Standards IC counters.
4. Interfacing counters with 7-segment LED /LCD display units.
5. Mux – Demux applications.

Note: Atleast ten experiments should be conducted in the semester, of which three should be from PART - B.

Suggested Readings:

1. D.Roy Chowdhary, B.Jain Shail - Linear Integrated circuit, 4th Edition.
2. Jain R.P., "Modern Digital Electronics" 3/e TMH 2003.

<table>
<tr><td>Course Code</td><td colspan="5">Course Title</td><td>Core / Elective</td></tr>
<tr><td>PC552EC</td><td colspan="5">SYSTEMS AND SIGNAL PROCESSING LAB</td><td>Core</td></tr>
<tr><td rowspan="2">Prerequisite</td><td colspan="4" rowspan="2">Contact Hours per Week</td><td rowspan="2">CIE</td><td rowspan="2">SEE</td><td rowspan="2">Credits</td></tr>
<tr><td rowspan="2">SATT
PC 304 EC
DSP
PC 503 EC</td><td>L</td><td>T</td><td>D</td><td>P</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>2</td><td>25</td><td>50</td><td>1</td></tr>
</table>

Course Objectives:

1. Implement the basic algorithms of DFT,IDFT,FFT and IFFT.
2. Design FIR Filter with specific magnitude and phase requirements.
3. Design IIR Filter with specific magnitude and phase requirements.
4. Describe the basics of Multirate signal processing.
5. Design and implement digital filters on DSP processors.

Course Outcomes:

1. Illustrate various signal processing algorithms.
2. Analyze FIR Filter with specific magnitude and phase requirements.
3. Analyze IIR Filter with specific magnitude and phase requirements.
4. Illustrate the basics of Multirate signal processing.
5. Analyze digital filters on DSP processors.

PART-A
Signal Processing Experiments

1. Introduction to Software used with details of some basics.
2. DFT andFFT algorithm.
3. Linear convolutions.
4. Circular Convolutions.
5. FIR filters design using different window functions.
6. IIR filters design: Butterworth and Chebyshev.
7. Interpolation and Decimation.
8. Implementation of multi-rate systems.
9. Time response of non –linear systems.
10. Design of P, PI, PD and PID controllers (any two)

PART-B
DSP Processor Experiments

1. Introduction to DSP processor kits and Software used with details of some basics.
2. Solution of difference equations.
3. Impulse Response.
4. Linear Convolution.
5. Circular Convolution.
6. Study of procedure to work in real-time.
7. Fast Fourier Transform Algorithms.
8. Design of FIR (LP/HP) USING windows: (a) Rectangular (b) Triangular (c) Hamming windows.
9. Design of IIR (HP/LP) filters.

NOTE:

1. Atleast ten experiments to be conducted in the semester.
2. Minimum of 5 from Part A and 5 from Part B is Compulsory.
3. For Section 'A' MATLAB with different toolboxes like signal processing,signal processing
4. Block set and SIMULINK / MATHEMATICA / any popular software can be used.

Suggested Reading:

1. Jaydeep Chakravorthy, ''Introduction to MATLAB Programming: Toolbox and Simulink",1/e, University Press,2014.

<table>
<tr><td>Course Code</td><td colspan="5">Course Title</td><td>Core / Elective</td></tr>
<tr><td>PC553EC</td><td colspan="5">INDUSTRIAL VISIT</td><td>Core</td></tr>
<tr><td rowspan="2">Prerequisite</td><td colspan="4" rowspan="2">Contact Hours perWeek</td><td rowspan="2">CIE</td><td rowspan="2">SEE</td><td rowspan="2">Credits</td></tr>
<tr><td rowspan="2">-</td></tr>
<tr><td>L</td><td>T</td><td>D</td><td>P</td><td></td><td></td><td></td></tr>
<tr><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>Grade</td><td>-</td><td>0</td></tr>
<tr><td colspan="8">Course Objective:

1. Able to assimilate and keep up abreast with the latest knowhow in the field of ECE Engineering
2. Able to articulate the observations they have made during their visit.
3. Demonstrate to skills of writing an engineering technical report.</td></tr>
</table>

Students are expected to visit at least two industries during the semester and submit a detailed technical report about the visit. The department should evaluate the reports through a committee consisting of two faculty members to award the grades listed below

Grade: Excellent / Very Good / Good/ Satisfactory / Unsatisfactory